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FISH & RICHARDSON P.C.
CITIGROUP CENTER 52ND FLOOR
153 EAST 53RD STREET
NEW YORK, NY 10022-4611

EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/876,554	IIDA, IZUO	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-15 and 17-24* is/are pending in the application.

4a) Of the above claim(s) *4-10,17 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,11-15 and 19-21* is/are rejected.

7)☒ Claim(s) *22-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 11-15 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komori et al. (U.S. Patent No. 5,656,522) in view of Hsieh et al. (U.S. Patent No. 6,165,845).

Komori et al. teaches in figure 4 and on column 5 lines 34-36 and column 8 lines 23-33, a method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate, the method comprising simultaneously forming the oxide film 8 on the floating gate 7a of the non-volatile memory cell transistor and a gate insulating film 8 of the MOS transistor in a single thermal oxidation step. Komori et al. does not teach selectively forming the oxide film on the floating gate or forming a tunneling insulating film over the gate insulating film and the oxide film.

Hsieh et al. teach a method of fabricating a poly tip in a split-gate flash EEPROM memory cell. Hsieh et al. teach selectively forming the oxide on the floating gate in figure 3f. Hsieh et al. also teach forming a tunneling insulator 50 (integrate layer 50 or interpoly, column 6 lines 8-10). Though the tunneling insulating film 50 is shown in

figure 2f, the method of forming it is not described. However, a similar film is formed in figure 3H. This film is labeled 170 and is disclosed as being formed by a blanket deposition step over the substrate. As is known in the art, a blanket deposition step deposits the layer over the entire substrate. In combining the references, it would be obvious that the tunnel insulating film of Hsieh et al. would be formed over the oxide film as Hsieh et al. teach depositing the tunnel insulating film over the entire substrate.

Komori et al. and Hsieh et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to selectively form the oxide film on the floating gate using the oxidation process taught by Hsieh et al. The motivation for combining the references is to provide a gate bird's beak to enhance Fowler-Nordheim tunneling for the programming and erasing of the cell and to form the tunneling insulator to insulate the control gate from the floating gate. Therefore, it would have been obvious to combine Komori et al. with Hsieh et al. to obtain the invention of claim 1.

With regard to claim 11, Komori et al. teach a method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate. Specifically, Komori et al. teach forming a silicon layer 7a on the substrate 1 (figure 3, column 8 lines 9-21), selectively removing the silicon layer on a region of the substrate where the MOS transistor is to be formed (figure 3, column 8 lines 9-21), and simultaneously forming an oxide film 8 on the region where the floating

gate is to be formed and a gate insulating film 8 on the region where the MOS transistor is to be formed (figure 4). Komori et al. do not teach forming an oxidation-resistant film over a first entire resulting surface, selectively removing the oxidation resistant film on the region of the substrate where the MOS transistor is to be formed and on a region of the substrate where the floating gate of the non-volatile memory cell transistor is to be formed, selectively forming the oxide film on the region where the floating gate is to be formed, or forming a tunneling insulating film over the gate insulating film and the oxide film.

Hsieh et al. teach a method of fabricating a poly tip in a split-gate flash EEPROM memory cell. Hsieh et al. teach forming an oxidation resistant film 50 over a first entire surface (figure 2b) and selectively removing the oxidation-resistant layer on the region where the floating gate of the non-volatile memory cell transistor is to be formed (figure 2c). Hsieh et al. then teach selectively forming an oxide film 45 on the region where the floating gate is to be formed (figure 2d) and forming a tunneling insulating film 50 over the gate insulating film 45 (figure 2f). Though the tunneling insulating film 50 is shown in figure 2f, the method of forming it is not described. However, a similar film is formed in figure 3H. This film is labeled 170 and is disclosed as being formed by a blanket deposition step over the substrate. As is known in the art, a blanket deposition step deposits the layer over the entire substrate. In combining the two references, it would be obvious to one of ordinary skill in the art a the time of the invention that the oxidation resistant film would be selectively removed on the region where the gate insulating film of the MOS transistor is to be formed as the process of Komori et al. teach forming the

oxide on the floating gate and the gate insulating film of the MOS transistor in the same oxidation step. Also, in combining the references, it would be obvious that the tunnel insulating film of Hsieh et al. would be formed over the oxide film as Hsieh et al. teach depositing the tunnel insulating film over the entire substrate.

Komori et al. and Hsieh et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form an oxidation resistant film on the entire surface and selectively remove the oxidation-resistant film where the floating gate is to be formed and where the MOS transistor is to be formed, to selectively form the oxide where the floating gate is to be formed, and to form a tunneling insulator over the gate insulating film and the oxide film. The motivation for combining the references is to provide a gate bird's beak on the floating gate to enhance Fowler-Nordheim tunneling for the programming and erasing of the cell and to form the tunneling insulator to insulate the control gate from the floating gate. Therefore, it would have been obvious to combine Komori et al. with Hsieh et al. to obtain the invention of claim 11.

With regard to claim 3, the oxidation resistant film of Hsieh et al. is taught as a silicon nitride film.

With regard to claim 12, the oxide film is formed by a single thermal oxidation step as taught by Komori et al.

With regard to claim 13, Komori et al. teach a method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate

stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate. Specifically, Komori et al. teach forming a gate insulating film 6 on the semiconductor substrate 1 (figure 2), forming a silicon layer 7a on the first gate insulating film 6 (figure 3, column 8 lines 9-21), selectively removing the silicon layer on a region of the substrate where the MOS transistor is to be formed (figure 3, column 8 lines 9-21), and simultaneously forming an oxide film 8 on the region where the floating gate is to be formed and a gate insulating film 8 on the region where the MOS transistor is to be formed (figure 4). Komori et al. do not teach forming an oxidation-resistant film over a first entire resulting surface, selectively removing the oxidation resistant film on the region of the substrate where the MOS transistor is to be formed and on a region of the substrate where the floating gate of the non-volatile memory cell transistor is to be formed, selectively forming the oxide film on the region where the floating gate is to be formed, removing at least some of the remaining oxidation-resistant film, or forming a tunneling insulating film over the gate insulating film and the oxide film.

Hsieh et al. teach a method of fabricating a poly tip in a split-gate flash EEPROM memory cell. Hsieh et al. teach forming an oxidation resistant film 50 over a first entire surface (figure 2b) and selectively removing the oxidation-resistant layer on the region where the floating gate of the non-volatile memory cell transistor is to be formed (figure 2c). Hsieh et al. then teach selectively forming an oxide film 45 on the region where the floating gate is to be formed (figure 2d), removing at least some of the remaining oxidation-resistant film (figure 2e) and forming a tunneling insulating film 50 over the gate insulating film 45 (figure 2f). Though the tunneling insulating film 50 is shown in

figure 2f, the method of forming it is not described. However, a similar film is formed in figure 3H. This film is labeled 170 and is disclosed as being formed by a blanket deposition step over the substrate. As is known in the art, a blanket deposition step deposits the layer over the entire substrate. In combining the two references, it would be obvious to one of ordinary skill in the art a the time of the invention that the oxidation resistant film would be selectively removed on the region where the gate insulating film of the MOS transistor is to be formed as the process of Komori et al. teach forming the oxide on the floating gate and the gate insulating film of the MOS transistor in the same oxidation step. Also, in combining the references, it would be obvious that the tunnel insulating film of Hsieh et al. would be formed over the oxide film as Hsieh et al. teach depositing the tunnel insulating film over the entire substrate.

Komori et al. and Hsieh et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form an oxidation resistant film on the entire surface, selectively remove the oxidation-resistant film where the floating gate is to be formed and where the MOS transistor is to be formed, selectively form the oxide where the floating gate is to be formed, remove at least some of the remaining oxidation-resistant film, and form a tunneling insulator over the gate insulating film and the oxide film. The motivation for combining the references is to provide a gate bird's beak on the floating gate to enhance Fowler-Nordheim tunneling for the programming and erasing of the cell and to form the tunneling insulator to insulate the control gate from the floating gate.

Therefore, it would have been obvious to combine Komori et al. with Hsieh et al. to obtain the invention of claim 13.

With regard to claim 14, the oxidation-resistant film of Hsieh et al. is taught as a silicon nitride film.

With regard to claim 15, the oxide film is formed by a single thermal oxidation step as taught by Komori et al.

With regard to claims 19-21, the selective oxidation step of Hsieh et al. teaches forming the oxide to a thickness of approximately 150 nanometers. In the combination of the two references, the gate insulating film of the MOS transistor is formed in the same oxidation step and would therefore have a similar thickness. Thus, the references as combined teach the gate insulating film being approximately 150 nanometers thick.

Allowable Subject Matter

3. Claims 22-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter: Prior art of record fails to teach the added limitation of claims 22-24, specifically, the prior art does not teach selectively etching the tunnel insulating film on the region of the semiconductor substrate where the MOS transistor is to be formed.

Response to Arguments

5. Applicant's arguments filed 7/28/04 have been fully considered but they are not persuasive.

Applicant has argued that the oxide film of Komori et al. is not formed simultaneously over the areas for the non-volatile memory element and the MISFETs. Applicant states that the different oxide films 8 are provided during different steps at different times. Applicant cites Komori et al. column 8 lines 23-33 in support of this argument. This argument is not persuasive as Komori et al. clearly states that that layer 8 (in the non-volatile memory element and the MISFETs) is formed in substantially the same step. By stating "by a manufacturing step substantially the same step, as this step, a second gate insulating film 8 is formed" Komori et al. is clearly stating that this is performed in the same step, not in a second step at a different time.

Applicant also argues that there would have been no motivation to combine selectively forming the oxide film of Hsieh et al. with Komori et al. In support of this argument applicant states that the gate insulating film 8 of Komori et al. remains over the entire area of the the MISFETs through many subsequent processing steps and thus, according to Komori et al., it is desirable to retain the insulating film 8 over the entire surface of the area of the MISFETs for many processing steps. First, Komori et al. do not explicitly teach retaining insulating film 8 over the area of the MISFETs through many subsequent processing steps. Komori et al. teach patterning to form gate electrodes 9 and then oxidizing the whole substrate to obtain the structure shown in figure 5 (column 8 lines 41-56). Komori et al. is silent as to whether insulating film 8 is

also etched during the etching to form gate electrodes 9, however, Komori et al. does explicitly teach oxidizing the entire substrate surface. Since Komori et al. is silent as to whether insulating layer 8 is removed or not, they do not teach an explicit or implicit desirability of leaving this layer through subsequent processing. Further, even if an insulator is desired, Komori et al. explicitly teach forming insulator 10 over the entire substrate such that if there is any desirability to having an insulator, one is directly provided in the oxidation to form insulator 10. Thus, removing insulating layer 8 would not be contrary to the techniques and teaching of Komori et al. Motivation for the combination was supplied in the rejection and as shown above, the combination is not contrary to the teachings of the references and as such the motivation is considered proper.

Applicant also argues that since Hsieh et al. relates to the fabrication of a memory cell alone, the combination of Hsieh et al. with Komori et al. would at most suggest using the techniques of Hsieh et al. in connection with the memory element, not the MISFETs. This argument is not persuasive to negate the rejection as applied. Hsieh et al. is only being relied upon to teach varying the process of Komori et al. by using an oxidation resistant film and selective oxidation on the memory element. Hsieh et al. is not being relied upon to change the process of Komori et al. for formation of the MISFETs.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NDR

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800